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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,138	03/11/2004	Andy Yu	M-16555 US	5554

32605 7590 12/26/2006
MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE
SUITE 400
SAN JOSE, CA 95110

EXAMINER

VU, DAVID

ART UNIT	PAPER NUMBER
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2818

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/26/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/798,138

Applicant(s)

YU ET AL.

Examiner

DAVID VU

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-20 is/are allowed.
- 6) ☒ Claim(s) 21-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 21-40 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hung et al. (US 6,765,260, hereinafter Hung) in view of Hong (US Pat. 5,427,968).

Regarding claims 21-24 and 26, Hung discloses in figs. 3G-3H an electrically erasable programmable memory device, comprising: a first semiconductor layer 200 doped with a first dopant in a first concentration (p-type); a second semiconductor layer 202, adjacent the first

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semiconductor layer 200, doped with a second dopant that has an opposite electrical characteristic than the first dopant (n-type), the second semiconductor layer having a top side; two spaced-apart diffusion regions 212/216 embedded in the top side of the second semiconductor layer, each diffusion region doped with the first dopant in a second concentration greater than the first concentration (col. 6, lines 4-25), the two diffusion regions including a first diffusion region 218a/218b and a second diffusion region 216, a first channel region defined between the first diffusion region 218a/218b and the second diffusion region 216; a floating gate 214a/214b, comprising a conductive material, disposed adjacent the first diffusion region 218a/218b and above the first channel region and separated therefrom by a first insulator region 212, the floating gate 214a/214b capable of storing electrical charge and having at least two lateral sides; and a control gate 208a/208b, comprising a conductive material, disposed laterally adjacent the floating gate 214a/214b and surrounding at least two sides of the floating gate (see fig. 6) and separated therefrom by a vertical insulator layer 212, the control gate 208a/208b being disposed above the first channel region and separated therefrom by a second insulator region 206a/206b.

Hung fails to disclose the control gate structure as recited in claim 21. However, Hong teaches in col. 4, lines 21-31 and figs. 4d&5d that the control gate 66 is disposed laterally adjacent the floating gate 60 on at least two sides of the floating gate 60 and separated therefrom by a vertical insulator layer 64, the control gate 66 being disposed above the channel region and separated therefrom by an insulator region 58. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Hung by forming

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the control gate structure as taught by Hong in order to increase the number of possible program/erase cycles for a memory cell (col. 4, lines 44-62).

Regarding claim 25, Hung discloses the first insulator region 212 having a thickness of about 90 angstroms (col. 5, lines 35-39).

Regarding claim 28, Hung discloses the floating gate 214a/214b and the control gate 208a/208b are wrapped by a spacer 212/210/220 (fig. 3H).

Regarding claims 29 and 35, Hung discloses the second diffusion 216 is in contact with a vertical connector 230, the vertical connector 230 being separated from the control gate 208a/208b by a second vertical insulator 212 (fig. 3H).

Regarding claim 27, Hong teaches in col. 3, lines 63-68 that the vertical insulator layer 64 is formed of ONO (figs. 4c-4d).

As for the recitation that “wherein charge is transported from the first channel region to the floating gate when a first combination of voltages is applied.....” (claims 30-34 and 36-40), it refers to an operational limitation and any such limitation must distinguish from the prior art in terms of structure rather than function, *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Allowable Subject Matter

2. Claims 1-20 are allowed.

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The following is an examiner's statement of reasons for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest an electrically erasable programmable memory device, comprising a control gate and a floating gate share a planarized top surface as instantly claimed and in combination with the remaining elements.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

3. Applicant's arguments with respect to claims 21-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on

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the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith S can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DAVID VU
PRIMARY EXAMINER